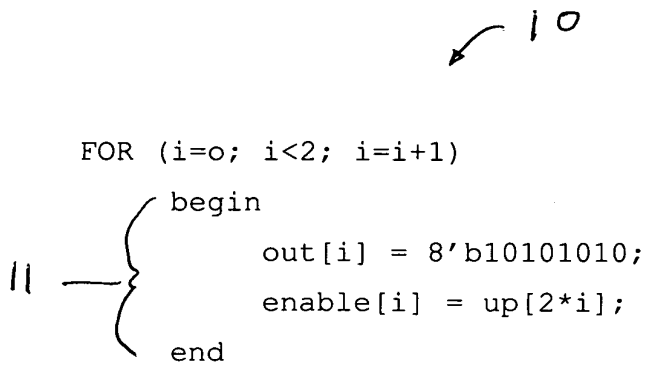

FIGURE 1

```
reg y [3:0];
WHILE (x <= y)
     begin
          fpl_bit[x+y] = mm_iru[x-y];
     end
```

13

12

FIGURE 2

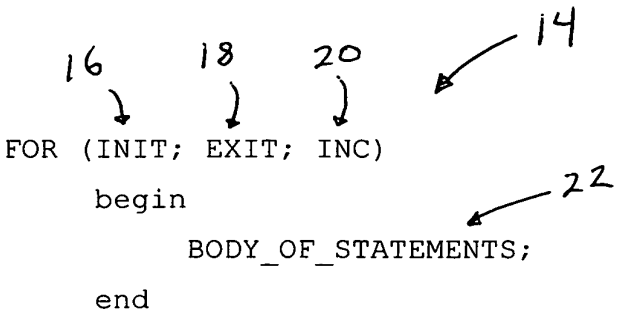

FIGURE 3

```
out[0] = 8'b10101010;
enable[0] = ~up[0];

out[0] = 8'b10101010;
enable[0] = ~up[2];
```

24

FIGURE 4

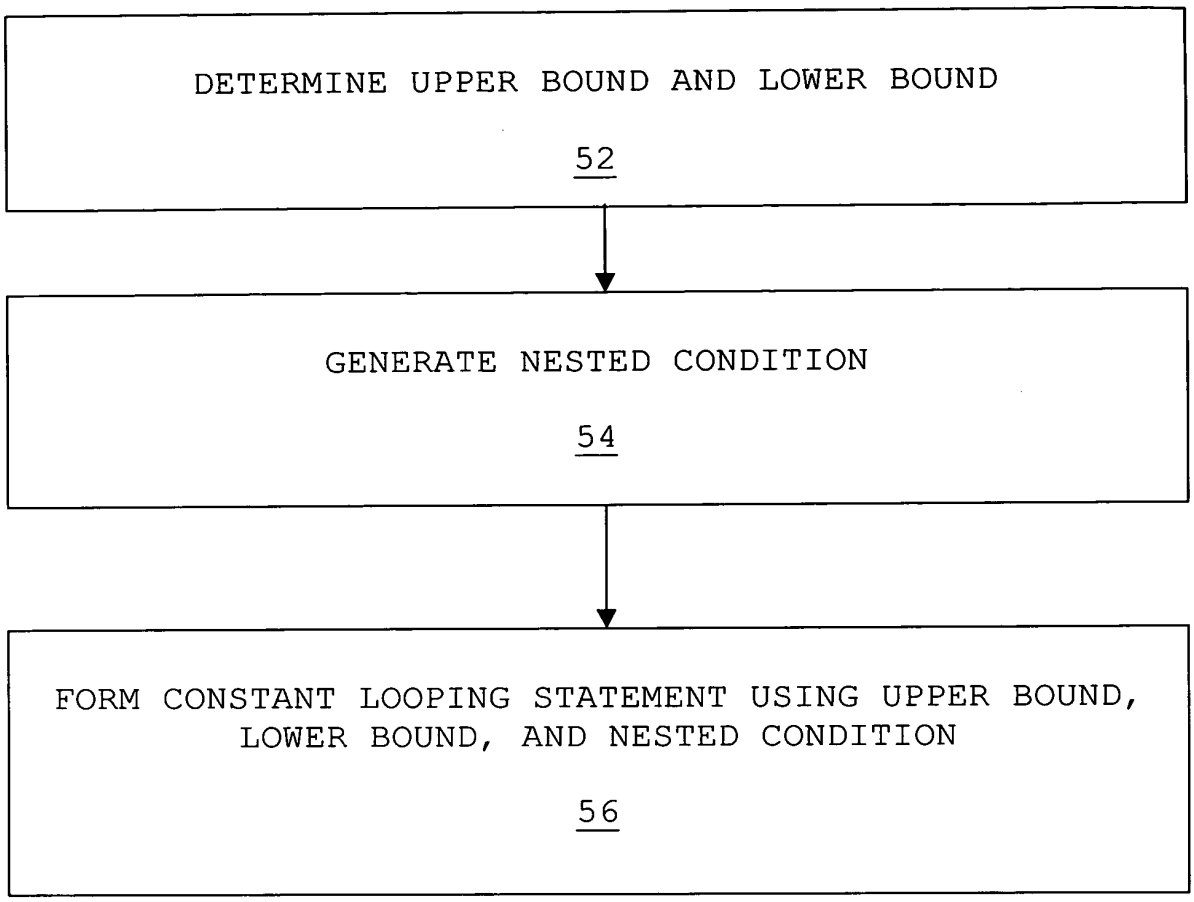

FIGURE 5

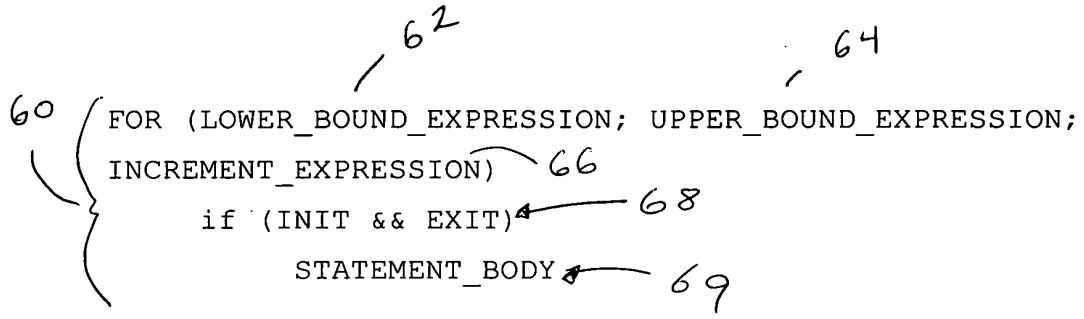
62
64
60
FOR (LOWER_BOUND_EXPRESSION; UPPER_BOUND_EXPRESSION;
INCREMENT_EXPRESSION)
66
if (INIT && EXIT)
68
STATEMENT_BODY
69

FIGURE 6

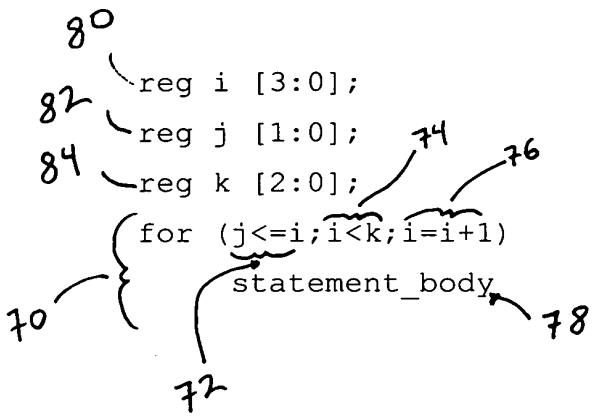
80
reg i [3:0];
82
reg j [1:0];
84
reg k [2:0];
74
76
for (j<=i;i<k;i=i+1)
statement_body
70
72
78

FIGURE 7

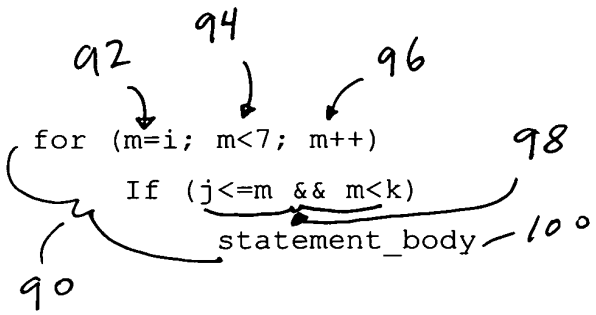

FIGURE 8

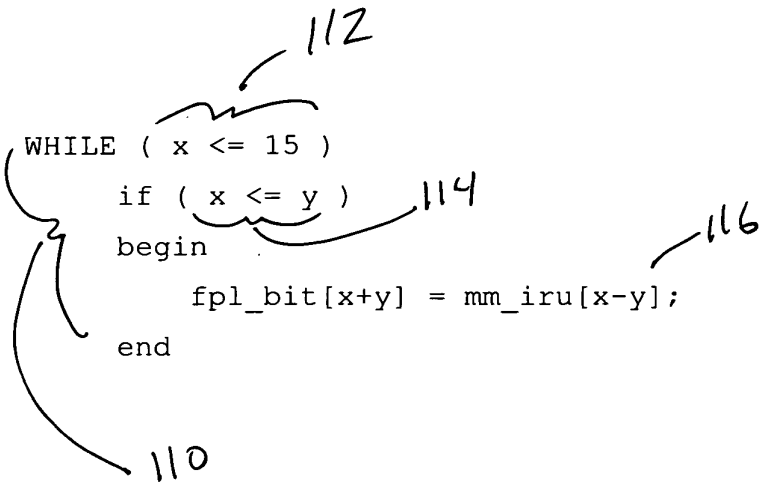

FIGURE 9